REMARKS

Claims 51, 52 and 54-69 remain in the application. Reconsideration of the application in view of the remarks to follow is requested.

Claims 51, 52 and 54-69 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Koh et al., U.S. Patent No. 5,686,337; or Chan et al., U.S. Patent No. 5,627,094; or Rosner, U.S. Patent No. 5,496,757; or Kim, U.S. Patent No. 5,403,767 or Summerfelt et al., U.S. Patent No. 5,619,393. Applicant traverses for at least the following five reasons.

I. Applicant's claimed subject matter.

Claim 51 recites "etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", which is not taught, disclosed, suggested or motivated by any of the cited references.

Claim 57 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 60 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming electrically insulative partitions between adjacent

capacitors after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 61 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming a second dielectric layer over the substrate, the second dielectric layer comprising a different material than the first dielectric layer; conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave partitions after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 62 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions", which is not taught, disclosed, suggested or motivated by the cited references.

Claim 66 recites "A method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings in a first dielectric layer; forming electrically insulative partitions between adjacent capacitors after etching the first capacitor container openings; and

anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions, the first and second capacitor container openings being formed on a common substrate", which is not taught, disclosed, suggested or motivated by the cited references.

The references each fail to provide the invention as recited in any of Applicant's claims. Additionally, the Office Actions fail to even attempt to relate the cited references to the invention as recited in Applicant's claims. For at least these reasons, the rejections of the claims are defective and should be withdrawn, and claims 51, 57, 60-62 and 66 and claims dependent therefrom should be allowed.

II. Unpatentability.

Unpatentability is a legal term of art. In order to make a valid finding of unpatentability, a number of legal concepts must be simultaneously satisfied.

A simple test for determining if elements suitable for a prima facie finding of unpatentability are present is set forth, for example, in the Manual of Patent Examination Procedure at §706.02(j), in a subsection entitled "Contents of a 35 U.S.C. 103 Rejection."

IIA. Lack of demonstration of motivation or suggestion.

Baldly listing or mis-stating teachings from references or modifying or augmenting teachings from one or more references, without demonstrating any relationship to the pending claims, does not meet appropriate standards

for a rejection under 35 U.S.C. §103(a). The prosecution history in the present application does no more than nakedly list various things purportedly taken from the references. There is no showing in the record of how these elements could possibly correspond to the subject matter recited in any of Applicant's claims, of how the teachings of the references could be modified or why one would do so.

Appropriate standards for a prima facie finding of unpatentability are set forth in The Manual of Patent Examination Procedure at §706.02(j), in a subsection entitled "Contents of a 35 U.S.C. 103 Rejection." This MPEP section states that three basic criteria must be met in order to establish a prima facie case of obviousness. The first of these is that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings.

The Office Action fails to show that the subject matter of any of claims 51, 52 and 54-69 is suggested or motivated by the teachings of any of the references. In fact, the Office Action is silent with respect to any reason to modify the teachings of any of the references. Put another way, the Examiner has not provided evidence of any shred of such motivation or suggestion, or, for that matter, modification of teachings, anywhere in the entire prosecution history!

IIB and C. Lack of expectation of success and of recited elements.

The second requirement of MPEP §706.02(j) is that there must be a reasonable expectation of success. The third requirement is that the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

IIC(i). Koh et al.

IIC(i)(a). The Koh et al. reference is silent with respect to forming an insulator intermediate two etching acts, as recited in claims 51, 60-62 and 66, or first and second anisotropic etching acts, as recited in claims 57, 60-62 and 66, the teachings of Koh et al. cannot possibly provide the invention as recited in any of Applicant's claims. As a result, there cannot possibly be a reasonable expectation of success from modifying the teachings of the Koh et al. reference.

The rejection of independent claims 51, 57, 60-62 and 66 as being unpatentable over Koh et al. fails all three components of the test for an obviousness rejection as set forth in the MPEP. For at least these reasons, the rejection of claims 51, 57, 60-62 and 66 should be withdrawn, and claims 51, 57, 60-62 and 66 should be allowed.

IIC(i)(b). Examiner's admission on the record regarding Koh et al.

The Examiner's rejection based on the teachings of the teachings of Koh et al. demonstrates on its face that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claims 51, 60-62 and 66. The

Examiner indicates (p.2) that the etching acts are shown in Figs. 3 and 5, while the insulative partitions are shown in Fig. 7, corresponding to a processing act subsequent to both of the etching acts. The Examiner restates this in the Conclusion (p. 3), noting that "Koh et al. clearly teaches an insulating layer formed between two capacitors after second etching."

To clarify this further, forming of a partition subsequent to two etching acts, as shown by Koh et al., is not equivalent to "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", as positively recited in claim 51. In other words, Koh et al. do not teach, disclose, suggest or motivate "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", and the Examiner fails to show any such step in Koh et al.

In fact, the Examiner's *Conclusion* in the Office Action dated June 26, 2001, and in the present Office Action, reiterates that Koh et al. do not teach or disclose the invention as recited in claim 51. The Examiner states (p. 4) that "Koh et al. clearly teaches an insulating layer formed between two capacitors after second etching." This is a repeated, explicit admission, on the record, that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claim 51.

Applicant specifically points out for the Examiner's benefit that teaching that something occurs after two etching steps does not teach something that occurs intermediate two etching steps. The word "intermediate" means "between", and does not mean or include "after".

To clarify this point yet further, a copy of p. 611 of the Merriam Webster's Collegiate Dictionary, 10TH Ed. (Merriam Webster, Springfield MA, copyright 1993, was enclosed in an Information Disclosure Statement together with the last Response. This page includes a definition of intermediate, viz., "beginning or occurring at the middle place, stage, or degree or between extremes". As such, it is abundantly clear that Koh et al. do not teach, disclose, suggest or motivate the invention as recited in claim 51. For at least these reasons, the rejection of claim 51 based on the teachings of Koh et al. is defective and should be withdrawn, and claim 51 should be allowed.

Claim 57 recites plural anisotropic etching steps. Koh et al. teach a first embodiment with respect to Figs. 2 and 5 using (col. 5, lines 36-40) one isotropic etching step, followed by one anisotropic etch of the same structure. Koh et al. not only fail to teach plural anisotropic etching steps, Koh et al. also do not teach etching of first and then second capacitor container openings, as recited in claim 57.

To clarify these concepts, Applicant has provided copies of pages 46 and 622 of Merriam Webster's Collegiate Dictionary, 10TH Ed. (Merriam Webster, Springfield MA, copyright 1993, in an Information Disclosure Statement that was included together with the last Response. The definition of "anisotropic" is "exhibiting properties with different values when measured in different directions". An anisotropic etch is an etch having a higher etch rate in one direction than in another.

The definition of "isotropic" is "exhibiting properties (as the velocity of light transmission) with the same values when measured along axes in all directions". An isotropic etch is an etch exhibiting the same etch rate in all directions (see, e.g., the dashed line in Fig. 3 of the Koh et al. reference).

Koh et al. teach a second embodiment with respect to Fig. 3 (see col. 6, line 4 et seq.). The second embodiment also fails to teach etching of first and then second capacitor container openings, as recited in claim 57. Koh et al. also do not teach first and second anisotropic etching steps with respect to the second embodiment. For at least these reasons, the rejection of claim 57 based on the teachings of Koh et al. is clearly defective and should be withdrawn, and claim 57 should be allowed.

Similarly, claims 60-62 and 66 provide an explicit ordering of etching, forming partitions and only then, following formation of the partitions, second etching. Again, the Examiner's own conclusion shows clearly that Koh et al. cannot possibly provide the invention as recited in these claims. Koh et al. teach formation of the partitions after both of the etching steps. For at least these reasons, the rejection of claims 60-62 and 66 based on the teachings of Koh et al. are clearly defective and should be withdrawn, and claims 60-62 and 66 should be allowed.

IIC(ii). Chan et al.

Chan et al. teach formation of a patterned planarized first dielectric layer 20b in a first anisotropic etching step (Fig. 2b; col. 8, lines 25-35). This step also defines capacitor container openings. As a result, Chan et al. do

not and cannot teach, disclose, suggest or motivate the invention as recited in claims 51, 60-62 and 66.

More specifically, Chan et al. teach formation of an insulator 20 (Fig. 2a). A patterned mask layer 24b is then formed (Fig. 2b; col. 7, lines 11-17). The insulator 20 is then etched to form dielectric layer portion 20b (Fig. 2b). The patterned portion 22b of the second dielectric layer is then completely etched (Fig. 2c and col. 8, line 57 through col. 9, line 6).

Because the dielectric layer portion 20b is formed during the first etching step and thus is shown clearly in Fig. 2b, it cannot be the result of "forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps", as recited in claim 51.

Claim 57 recites first and second anisotropic etching steps. The second etching step taught by Chan et al. is an isotropic etching step (col. 8, lines 61 and 62). The undercutting needed to remove the portion 24b cannot be carried out using anisotropic etching. Similarly, claims 60-62 and 66 provide an explicit ordering of anisotropic etching, forming partitions and only then, following formation of the partitions, second anisotropic etching.

As a result, Chan et al. do not and cannot teach, disclose, suggest or motivate the invention as recited in claims 51, 57, 60-62 and 66. Because Chan et al. fail to provide the elements recited in Applicant's claims, there can be no reasonable expectation of success from modification of Chan et al. to attempt to arrive at Applicant's claimed subject matter. The rejection based on Chan et al. fails all three prongs of the test for unpatentability found in the MPEP. For at least these reasons, the rejections of claims 51, 57, 60-

62 and 66 based on the teachings of Chan et al. are defective and should be withdrawn, and claims 51, 57, 60-62 and 66 should be allowed.

IIC(iii)(a). Rosner.

Rosner does not teach or disclose formation of an insulative partition intermediate two etching steps, as recited in claim 51. Additionally, Rosner teaches (col. 5, lines 54 and 55) that "The first auxiliary layer 4 is then removed by wet-chemical etching using, for example, choline." Wet etching of polysilicon layer 4 (col. 5, line 17) is, by definition, isotropic etching. Accordingly, Rosner does not teach first and second anisotropic etching acts, as is recited in each of claims 60-62 and 66.

Claims 57, 60-62 and 66 each clearly recite an ordered sequence of acts such as (i) anisotropic etch, (ii) formation of insulator and (iii) anisotropic etch. In contrast, the Examiner's bald recitation of teachings from Rosner indicates that Rosner teaches an ordered sequence of acts such as (i) etch, (ii) isotropic etch and subsequent (iii) insulator formation.

Further, the Office Action does not contain any statement or effort to relate this disclosure to the subject matter of any of Applicant's claims. As a result, Rosner does not and cannot teach, disclose, suggest or motivate the invention as recited in claims 57, 60-62 and 66.

Because Rosner fails to provide all of the affirmatively-recited acts of Applicant's claims, there cannot possibly be a reasonable expectation of success from modification of the teachings of the Rosner reference. The

rejection of claims 51, 57, 60-62 and 66 fails all three components of the test for unpatentability set forth in the MPEP.

For at least these reasons, the rejection of claims 51, 57, 60-62 and 66 based on the teachings of the Rosner reference is defective and should be withdrawn, and claims 51, 57, 60-62 and 66 should be allowed.

IIC(iii)(b). Examiner's admission on the record regarding Rosner.

The Examiner's rejection based on the teachings of Rosner demonstrates on its face that Rosner does not teach, disclose, suggest or motivate the invention as recited in any of claims 51, 57, 60-62 and 66. The Examiner indicates (p. 3) that the etching acts are shown in Figs. 3-5, while formation of the insulative partition is shown in Fig. 6, corresponding to a processing act subsequent to the etching acts. For at least these reasons, the rejection based on Rosner is clearly defective and should be withdrawn, and claims 51, 57, 60-62 and 66 and claims dependent therefrom should be allowed.

IIC(iv). Kim

Kim '767 teaches etching first openings in an insulating layer 7 in Fig. 1C. The first openings are not capacitor container openings. Kim '767 then teaches formation of "second insulating film spacers 8A" followed by formation of "etching barrier layer 9" (Fig. 1D; col. 2, lines 42-57). Kim '767 teaches formation of capacitor containers in Fig. 1E by removal of the reminder of the insulating layer 7A, i.e., in a single etching step. As a result,

Kim '767 does not and cannot teach, disclose, suggest or motivate formation of insulative partitions between two separate etching steps, as recited in claim 51.

Further, because Kim does not teach anisotropic etching until Fig. 2A (col. 3, lines 37-44), the cited portions of Kim cannot possibly teach, disclose, suggest or motivate the invention as recited in any of claims 57, 60-62 and 66. Because Kim fails to provide the elements recited in Applicant's claims, there can be no reasonable expectation of success from modification of Kim to attempt to arrive at Applicant's claimed subject matter. The rejection based on Kim fails all three prongs of the test for unpatentability found in the MPEP.

For at least these reasons, the rejection of claims 51, 57, 60-62 and 66 based on the teachings of Kim is defective and should be withdrawn, and claims 51, 57, 60-62 and 66 should be allowed.

IIC(v). Summerfelt et al.

The Examiner first makes reference to Figs. 25+ and then states that Summerfelt teaches etching insulating layer 70 in Fig. 1E. Summerfelt has no Fig. 1E. Clarification is requested.

Summerfelt et al. teach formation of what will later become capacitor dielectric layers 56 using BST (barium strontium titanate) in Figs. 25-28 (see also col. 8, line 36 through col. 9, line 8). A first capacitor electrode is formed atop conductive plug 52, using a platinum layer 74 and a conductive titanium nitride layer 76 (fig. 29; col. 9, lines 8-14). Portions of these

conductive layers 74 and 76 formed atop the BST pillars 56 are then removed (Fig. 31; col. 9, lines 16-21).

As a result, an outer electrode comprising platinum 60 and titanium nitride 64 is formed on an outer surface of the capacitor dielectric 56, and an inner electrode comprising platinum 58 and titanium nitride 62 is formed within an inner surface of the capacitor dielectric 56. As noted by Summerfelt et al. (col. 9, lines 26-28), "As can be seen in FIG. 31, the outer electrode can be made common between e.g., all capacitors in a DRAM." As a result, it is apparent that the outer surface of the capacitor dielectric 56 cannot possibly form a second capacitor container, as alleged in the Office Action. For at least these reasons, the rejection of claims 51, 52 and 54-65 over Summerfelt et al. is clearly in error and should be withdrawn, and claims 51, 52 and 54-56 should be allowed.

Claim 57 recites "a method of forming a plurality of DRAM capacitors comprising: anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate."

Summerfelt et al. provide no teaching at all of first and second capacitor container openings. The Office Action is also silent with respect to the invention as recited in claim 57.

Summerfelt et al. teach anisotropic ion milling of platinum (col. 7, lines 63-65). Summerfelt et al. also teach anisotropic etching of BST to form capacitor dielectric layer 56 (col. 8, lines 56-60). Summerfelt et al. make no further mention of anisotropic etching. As a result, it is inconceivable that

Summerfelt et al. could possibly teach, disclose, suggest or motivate the multiple anisotropic etching steps recited in each of claims 57, 60-62 and 66.

Because Summerfelt et al. fail to provide the elements recited in Applicant's claims, there can be no reasonable expectation of success from modification of Summerfelt et al. to attempt to arrive at Applicant's claimed subject matter. The rejection based on Summerfelt et al. fails all three prongs of the test for unpatentability found in the MPEP.

For at least these reasons, the rejection of claims 51, 57, 60-62 and 66 is in error and should be withdrawn, and claims 51, 57, 60-62 and 66 should be allowed.

III. Modification cannot defeat intended purpose

Attempting to adapt the teachings of Chan et al. to arrive at the subject matter recited in claims 57, 60-62 and 66 defeats the main intent of Chan et al. and also makes the teachings of Chan et al. unsuitable for their intended purposes. It is improper to modify the teachings of a reference in such a manner (see MPEP §§ 2145(X), 2141.02 and 2143.01).

More specifically, the second etching step taught by Chan et al. is an isotropic etching step (col. 8, lines 61 and 62). The undercutting needed to remove the portion 24b cannot be carried out using anisotropic etching. Claim 57 recites first and second anisotropic etching steps. Similarly, claims 60-62 and 66 provide an explicit ordering of anisotropic etching, forming partitions and only then, following formation of the partitions, second anisotropic etching.

Because substitution of Applicant's affirmatively-recited acts into the teachings of Chan et al. renders it impossible to achieve the undercutting needed by Chan et al., the teachings of Chan et al. are rendered unsuitable for their intended purpose if modified to arrive at Applicant's claimed subject matter. Such also defeats the main intent of Chan et al.

Applicant notes the requirements of MPEP §2143.01, entitled "Suggestion or Motivation to Modify the References". This MPEP section states that "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE". This MPEP section further states that "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)."

Accordingly, there is no suggestion or motivation, as a matter of law, to modify the teachings of Chan et al. to attempt to arrive at the subject matter of any of Applicant's claims. For at least these reasons, the rejection of claims 57, 60-62 and 66 should be withdrawn, and claims 57, 60-62 and 66 should be allowed.

IV. Dependent claims.

Dependent claims 52, 54-56, 58, 59 and 63-65 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

For example, claim 55 recites that "etching capacitor container openings comprises: anisotropically etching first capacitor container openings in a first etching step; and anisotropically etching second capacitor container openings in a second etching step", while claim 56 recites that "etching capacitor container openings comprises: anisotropically etching first capacitor container openings; and anisotropically etching second capacitor container openings", which is not taught, disclosed, suggested or motivated by any of the cited references, and which further appears nowhere in the Office Action.

V. Lack of Evidence for motivation

Further, no evidence has been provided as to why it would be obvious to modify the teachings of any of these references. Evidence of a suggestion to combine or modify may flow from the prior art references themselves, from the knowledge of one skilled in the art, or from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

VI. Examiner deficiencies.

The Examiner's response to argument is deficient in multiple regards, and several formal matters have not been addressed. This is explained below in more detail.

VI(i). A first deficiency is that the response to argument clearly fails to respond to Applicant's arguments with respect to the rejections under 35 U.S.C. §103, or, in the alternative, is an admission that these rejections are defective.

Applicant notes the requirements of MPEP §707.07, entitled "Completeness and Clarity of Examiner's Action". This MPEP section cites 37 CFR §1.104, entitled "Nature of examination" which in turn states, in subsection (b), entitled "Completeness of examiner's action" that "The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made."

This MPEP section further states, under a heading labeled "Examiner Note" that "The Examiner must, however, address any arguments presented by the applicant which are still relevant to any references being applied." The Office Action clearly fails to comport with these requirements as set forth in the MPEP, at least because the Office Action both fails to address Applicant's arguments with respect to anticipation and continues to reject claims as being anticipated.

VI(ii). A second deficiency is that under the unpatentability rejections, the combinations fail to provide all of the features recited in any of Applicant's independent claims (see MPEP §706.02(j) for criteria for establishing a prima facie case of unpatentability). The Examiner has

ignored these features without providing any appropriate legal basis for doing so.

VI(iii). A third deficiency is the failure to respond to all arguments traversing the unpatentability rejections. Merely repeating various elements taught by the references with no effort at all to provide the features recited in the claims does not constitute a basis for rejection of the claims. This is particularly true when the references fail to provide the features recited in the claims and the rejections fail to meet the standards for such rejections as set forth in the MPEP and as demonstrated by Applicant.

VI(iv). A fourth deficiency is the failure to return initialed form PTO-1449 forms to Applicant. Specifically, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO 1449 filed in this application on September 26, 2001, together with the last Response. No initialed copy of the PTO-1449 has been received back from the Examiner.

To the extent that the submitted references listed on the Form PTO 1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

VI(v). A fifth deficiency is a failure to advise Applicant of the status of the drawings. Formal drawings were filed in this Application on

October 21, 1999. None of the three Actions to date have provided any indication of the status of the drawings. Clarification is requested.

For at least these reasons, the Office Action fails to comport with appropriate standards for examination. The Examiner should either allow Applicant's claims or provide a meaningful basis for rejection and an appropriate response to Applicant's arguments.

In order to assist the Examiner in identifying the arguments in order to respond to them, Applicant has specifically enumerated them. The Examiner should either allow Applicant's claims or provide meaningful rebuttal to each of arguments **I, II, IIA, IIC(i)(a), IIC(i)(b), IIC(ii), IIC(iii)(a), IIC(iii)(b), IIC(iv), IIC(v), III, IV, V** and **VI(i)-(v)**.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

In view of the foregoing, allowance of claims 51, 52 and 54-69 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Apr. 11, 2002 By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/420,635
Filing Date ..... October 21, 1999
Inventor ..... Werner Juengling
Assignee ..... Micron Technology, Inc.
Group Art Unit 2812
Examiner ..... H. Tsai
Attorney's Docket No. MI22-1243
Title: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY
RESPONSE TO DECEMBER 12, 2001 OFFICE ACTION

Deletions are bracketed, additions are underlined.

There are no amendments to the specification or claims.

END OF DOCUMENT